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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,621	06/09/2000	Vidyabhusan Gupta	99-LJ-186	3053

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EXAMINER	
ROSALES HANNER, MORELLA I	
ART UNIT	**PAPER NUMBER**
2123	2

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/591,621	GUPTA, VIDYABHUSAN
	Examiner	Art Unit
	Morella I Rosales-Hanner	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *09 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1.1 **Claims 1 – 28** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no support in the Applicant's specification for:

- a Simulation Controller,
- a Memory Access Monitor or,
- a Memory Optimization Controller

Such that one of ordinary skills in the art without undo experimentation could make and/or use the Applicant's claimed invention.

The Examiner's motivation for this rejection is based on the information disclosed on a technical report from the Department of Computer Science & Engineering of the Indian Institute of Technology in Delhi titled: "Processor Evaluation in an Embedded Systems Design Environment" written by Gupta et al.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2.1 Claims 1, 2, 5, 7, 8, 9, 12, 14, 15 – 22, 23, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over article "Processor Evaluation in an Embedded Systems Design Environment" written by Gupta et al. hereafter referred to as *Gupta,* in view of US Patent No. 6,263,302 B1 issued to Hellestrand et al., hereafter referred to as *Hellestrand.*

2.1.1 In regard to **claims 1, 8, and 15 – 22,** the *Gupta* reference discloses:

a Memory Bandwidth Requirement module **[section 5.4 of page 25]** that takes an analyzed version of a user program and iterates over all the instructions, within a block of code, and keeps track of the number of operations to determine the I/O intensity of the user program, which is equivalent to applicant's memory access monitor;

an Estimator module **[page 6, figure 2.1]** that: takes as input an intermediate representation of a given user program as well as a set of parameters that characterize the processor architecture or predetermine design criteria, outputs an architecture that would be best suited for the given user program, which is equivalent to the applicant's memory optimization controller;
a set of software modules and applications that were developed and integrated to create an environment for processor evaluation, which is equivalent to the applicant's processing system claimed in claim 22.

Gupta fails to explicitly disclose a simulation controller that is capable of simulating execution of a user program.

However, Hellestrand discloses **[column 9, line 52]** a Processor Simulator, capable of simulating execution of a user program on a target processor by executing an analyzed version of the user program. The analyzed version is derived from the user program by an analysis process. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the modules disclosed by *Gupta* with the processor Simulator disclosed by Hellestrand to automate the simulation of application-specific software in order to improve efficiency and lower the cost of embedded systems design.

2.1.2 In regard to **claims 2, 9, and 23,** *Gupta* discloses an Estimator module **[page 6, figure 2.1]** that: takes as input an intermediate representation of a user program as well as a set of parameters that characterize the processor architecture or predetermined design criteria; and outputs an architecture that would be best suited for the given user program;

Gupta fails to explicitly disclose the details of the identified architecture such as memory types such as static random access memory (SRAM), dynamic random access memory (DRAM) read-only memory (ROM), random access memory (RAM), flash (FLASH), and electronically erasable programmable read-only memory (EEPROM).

However, *Hellestrand* discloses **[column 30, line 5]** a target link map that is generated to use in each simulation and that contains a default allocation where all code and all constants are mapped into non-volatile memory such as ROM, while all data areas as well as the heap and stack are mapped into volatile memory such as RAM. *Hellestrand* also states **[column 30, line 10]** that means are provided for other memory allocation alternatives. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the Estimator module disclosed by *Gupta* to provide allocation of different memory types as disclosed by *Hellestrand* in order to determine a suited memory configuration from a set of the most commonly used volatile memory types (e.g., registers, cache, RAM) and non-volatile memory types (e.g., ROM, EEPROM, flash memory, etc.), or some combination of the two.

2.1.3 In regard to **claims 5, 12 and 26,** *Gupta* discloses **[Chapter 7]** results generated by running the parameter extractor on some code indicating some characteristics of the user program such as: percentage of cycles having a particular number of load/store operations, address computation operations and, data computational operations. *Gupta* discloses **[page 32, paragraph 3]** that there is a lot of variation in all the parameter values.

Gupta fails to disclose explicitly that the amount of variation in all the parameter values presented in the results could be improve by running the user program a number of times and applying statistical analysis to the results.

Hellestrand discloses under the Cache Modeling and Memory System Simulation section [**column 14 line 43**] a simulator that reports global run-time statistics about the performance of a program as well as statistics of the individual basic linear blocks of the user program.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the parameter extractor disclosed by *Gupta* to run the user program a number of times to obtain more run-time statistics about the user program and apply statistical analysis, as disclosed by *Hellestrand,* in order to provide more accurate results.

2.1.4 In regard to **claims 7, 14 and 28,** *Gupta* discloses **[Chapter 3 page 8]** that the Stanford University Intermediate Format (SUIF) tool, which was used to build the Estimator module, is well suited for optimization and for code generation.

The *Gupta* reference fails to explicitly disclose an optimization controller capable of modifying a user program in response to its memory usage and one or more predetermined design criteria.

However, *Hellestrand* discloses **[Column 14 line15]** a simulator that is capable of identifying the location of any bottleneck of the analyzed user program making it useful for tuning the user program. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the Estimator component disclosed by *Gupta* to use the optimization and code generation capabilities of the SUIF tool to tune the user program as disclosed by *Hellestrand* in order to produce a version of the user program that is optimized to meet its memory usage needs along with one or more predetermined design criteria.

2.2 Claims 3, 4, 10, 11, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Gupta* in view of US Patent No. 6,604,067 B1 issued to Abraham et al. hereafter referred to as *Abraham.*

Gupta discloses **[section 1.1 page 3]** a design methodology for embedded systems that, used in conjunction with a given system specification along with the disclosed tools which were developed to support the methodology, will synthesize a system that meets the specification constraints.

Gupta fails to disclose specific details of the architecture of the synthesized system.

However, the *Abraham* reference discloses **[column 2, line 42]** a system, which simplifies and speeds up the process of designing a computer system by evaluating the components of the memory hierarchy for any member of a broad family of processors in an application–specific manner. *Abraham* teaches **[column 1, line 59]** that in general, an embedded computer system consists of a processor, and associated Level-1

instruction, Level-1 data, and Level-2 unified caches, and main memory and that in an embedded system, the system performance, memory and arithmetic capabilities are all adjusted to exactly match its dedicated task needs. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the resulting synthesized system disclosed *Gupta* to include specific memory configurations as suggested by *Abraham* in order to optimize the design of an embedded system.

2.3 Claims 6, 13 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Gupta* in view of US Patent No. 6,052,524 issued to Mark R. Pauna referred to hereafter as *Pauna.*

Gupta discloses **[Chapter 7 of page 32]** estimation results, which are output by the parameter extractor, showing how parameters from the analyzed user program can vary when compared to a range of target processors. *Gupta* further discloses that the range of these parameters is substantial and can help in selecting/rejecting processors in performance critical applications. *Gupta* discloses results of the cycle count parameter **[page 34, Table 7.1]** and notes how there is a difference in the cycle count parameter of 30% to 200% between two different processors.

Gupta fails to explicitly disclose performance results specific to memory configuration.

However, *Pauna* teaches **[column 2 line 38]** that one of the most common and underestimated problems associated with the design of an embedded system is its memory interaction since the speed and structure of memory usually has a significant impact on the performance of an embedded system. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the results of the parameter extractor disclosed by *Gupta* in view of *Pauna* to determine a memory configuration best suited for an embedded system in order to address one of the most underestimated problems associated with the design of embedded systems.

Response Guidelines

3. A shortened statutory period to response to this action is set to expire 3 (**three**) months and 0 (zero) days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02, 710.02(b)).

3.1 Any response to the Examiner in regard to this non-final action should be directed to:

Morella Rosales-Hanner
telephone number (703) 305-8883
Monday-Friday from 7:00 a.m. to 3:30 p.m. ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. Any inquiry of a general nature should be directed to the Technology Center (TC) 2100 receptionist, telephone number (703) 305-3900. The TC 2100 receptionist, telephone number (703) 306-5631.

Mailed to: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or faxed to: (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121Crystal Drive, Arlington, VA, Fourth Floor (Receptionist)

Morella Rosales-Hanner
October 27, 2003

RUSSELL FREJD
PRIMARY EXAMINER